AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An output filter for a delta sigma modulator, comprising:

a constant current source;

~~an~~ FIR filter having a plurality of delay element arranged in cascade, each element being operative to ~~that outputs~~ output data of ~~a~~ the delta sigma modulator ~~from each of plural delay elements cascaded, controls~~ by controlling currents from ~~a~~ the constant current source on the basis of each of the output data to thereby ~~attain~~ generate a plurality of weighted currents that are weighted according to a filter characteristic, ~~and adds~~ the weighted currents being added and outputted at an output side of the FIR filter ~~to output the result, wherein:~~

~~the current source is a constant current source~~.

2. (currently amended): An output filter for a delta sigma modulator as claimed in Claim 1, further comprising a current-to-voltage conversion unit, said unit having an input side coupled to the output side of the FIR filter and comprising ~~that performs the current-to-voltage conversion by feedback resistors of~~ a full differential operational amplifier and feed back resistors, said amplifier having an ~~on the~~ output side ~~of the FIR filter~~.

3. (original): An output filter for a delta sigma modulator as claimed in Claim 2, further comprising a single differential conversion operational amplifier on the output side of the full differential operational amplifier.

4. (original): A digital signal processor comprising an output filter for a delta sigma modulator, as claimed in any of Claim 1 to Claim 3.

5. (new): An output filter for a delta sigma modulator as claimed in Claim 1, wherein each said delay element comprises a flip-flop and a respective pair of MOS transistors.

6. (new): An output filter for a delta sigma modulator as claimed in Claim 5, wherein said flip flop generates two outputs and each said output is coupled to a gate of a respective one of the MOS transistors.

7. (new): An output filter for a delta sigma modulator as claimed in Claim 1, wherein said constant current source comprises a common source for generating said plurality of weighted currents.